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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEE, EUGENE	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/467,141	MA ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,21-29 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,21-29 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 thru 4, 7 thru 18, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohda et al. '999 in view of Tigelaar '926. Kohda discloses (see, for example, FIG. 3A) an EPROM cell (cell structure) comprising impurity regions (first and second junction) 2/3, channel region, first and second floating gates 4a/4b, control gate (select-gate) 6, interlayer insulation films 7a/7b, gate insulation film 8 and substrate (body region) 1. The operation of the cell is determined by the voltages applied to the source, drain, substrate and control gate. Regarding claim 26, see FIG. 7. Kohda does not disclose the select-gate extending across the entire length of each of the first and second junctions. However, Tigelaar discloses (see, for example, FIG. 3e) a memory cell comprising a source region (first junction) 74, drain region (second junction) 76, channel 72, floating gate elements (first and second floating gates) 60a/60b, control gate (select-gate) 90, and insulation layer (insulating layer) 80. The control gate 90 extends across the entire length of the source and drain region. The control gate serves as a column line that accesses the memory cells of an array. See, for example, column 5, lines 25-39 of Tigelaar. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the select-gate extend across the entire length of each of the first and second junctions in order to form a column line that can access the memory cells of an array.

3. Claims 5, 6, 21 thru 24, 27 thru 29 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohda et al. '999 in view of Tigelaar '926 as applied to claims 1 thru 4, 7 thru 18, 25, and 26 above, and further in view of Guterman '691. Kohda in view of Tigelaar does not disclose the first and second floating having at least one slanted surface forming a sharp edge. However, Guterman shows (see, for example, FIG . _1) an EEPROM memory device comprising a floating gate 120, programming electrode 110 and tunneling element 101. Guterman teaches (see, for example, column 4, lines 19-42) that microtexturing the floating gate will enhance the local electric field and facilitate tunneling at lower voltages. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have at least one slanted surface forming a sharp edge in the floating gates of Kohda in view of Tigelaar so that one can enhance the tunneling of electrons from the floating gate through the insulation film to the control gate.

Regarding claims 23 and 24, the floating gates being bowl-shaped does not provide any critical or unexpected results to the cell structure's operation. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it in not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F. 2d 454, 456 105 USPQ 233, 235 (CCPA 1995).

Response to Arguments

5. Applicant's arguments filed 5/28/03 have been fully considered but they are not persuasive.

Regarding applicant's argument on page 2, second paragraph that the patent drafteee of the Tigelaar et al. patent mistakenly matched up control gates 90 in FIG. 5e with column lines 16 in Fig. 1 instead of with row lines 12, and conversely mistakenly matched up source and drain regions with row lines 12 instead of column lines 16, the Examiner respectfully disagrees. The applicant has not shown any evidence why this is a drafting error except stating "It is notoriously well known in this art that in semiconductor memory arrays, gates of memory cells form row lines which are coupled to a row decoder, and drain and source regions of memory cells form column lines which are coupled to a column decoder." Therefore, the statement carries no weight. However, even if this statement were true, row lines and column lines are functionally and structurally identical to each other that it would make no difference whether the control gates were matched with either row lines or column lines.

Regarding the applicant's argument on page 3, middle paragraph that extending control gate 6 over drain and source regions 2, 3 prevents column lines from contacting the drain and source regions, the Examiner respectfully disagrees. Tigelaar clearly shows (see FIG. 3e) control gates 90 that extend over drain and source regions 74, 76 without contacting the drain and source regions. Therefore the same structure that is shown in Tigelaar may be applied to Kohda by having Kohda's control gate extend over drain and source regions without contacting the drain and source regions.

Regarding the applicant's argument on page 3, last paragraph that the source and drain regions would no longer be self-aligned to the edges of control gate 6 and make the cell susceptible to process misalignments, the Examiner respectfully disagrees. The edges of the source and drain regions may be aligned to the control gate by various methods that do not misalign the control gate and source and drain regions. For example, the vertical nature of the control gate 6 may be laid down which aligns the source and drain regions. Afterwards, the horizontal nature of the control gate may be laid down without affecting the alignment between the source and drain regions and the control gate.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
August 7, 2003

B. WILLIAM BAUMEISTER
PRIMARY EXAMINER